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Engineering high aspect-ratio silicon nanostructures

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There has been huge interest in synthetizing silicon nanomaterials for various applications ranging from electronics to biology due to their attractive properties. For many device applications, it is pivotal to control the morphology and dimensions of silicon-based nanomaterials while considering a continuous demand for higher resolution and large aspect ratio. Such prerequisites concomitant with scalability, reliability, low cost and compatibility with existing manufacturing processes are not trivial to fulfill, bringing a need to develop nanofabrication techniques. In this regard, the work proposed in this paper involves the advancement of a top-down fabrication approach called "Metal-assisted Chemical Etching (MACE)" which has the potential to overcome the current limitations of 1D and 3D semiconductor nanomanufacturing processes. Large-area high density vertical silicon nanowire arrays are fabricated by this technology. Two-dimensional silica colloidal crystal template or laser interference lithography are used to create gold metal nanohole arrays on a silicon substrate, which enables to precisely control the final diameter of the nanowires. The formation of ordered silicon nanowire arrays is due to selective and highly anisotropic etching of silicon induced by the gold patterned mask.

Key words: Silicon nanowire, metal-assisted chemical etching, nanosphere lithography, laser interference lithography
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Introduction

Crystalline silicon (c-Si) is the leading material for the electronics and photovoltaics industries today. This salient position proceeds from a unique combination of electronic [1], electro-mechanical [2], thermo-electric [3], optical [4], and electro-optic [5] properties. Integration and economy of scale are the two major elements in the technological achievement of Si. The huge abundance on earth combined with its low-cost, the silicon is tremendously valuable compared to other semiconductors. Furthermore, its optimal band gap (1.12 eV) for room temperature operation, the stability, the easy and finely controlled realization of silicon oxide, favors the processing flexibility to integrate more than 10^8 transistors on a single chip. These properties have enabled the electronics industry to follow Moore's law for over four decades, pushing the development of silicon technology to its present maturity. This yields incredible processing capability and high-speed device performance. The device downsizing involves longer, more power- and time-consuming interconnections, in addition to a more complex circuit design. The interconnection bottleneck due to RC delays is already existent today. New physical phenomena demonstrated at the nanoscale promoted the emerging of Si based nanostructures for tomorrow's technologies. The investigation of nanostructures unveils distinct characteristics and subsequently many advantages for practical applications compared to their bulk counterparts [6]. When the size of structures attains the nanoscale, the ratio of surface to volume builds up drastically and consequently the physicochemical properties of nanomaterials are modified and can be adjusted by surface effects. In the past decade, a significantly amount of developments has been made in the field of one-dimensional nanostructures. In particular, silicon nanowires (Si NWs) have proven to be good candidates for applications in nanoscale electronics [7], ultrasensitive sensors [8], photovoltaics [9], photonics [10], and a variety of other devices. The ability to decrease their lateral dimensions down to

diameters comparable or smaller than characteristic lengths, including the wavelength of photons, the mean free path of phonons, and the diffusion lengths of photoexcited carriers [11], leads to unique features observed in the physical properties of the nanowires, which have been reported in different subdisciplines of physics and chemistry [12]. Consequently, it is critical to synthesize SiNWs with controlled diameter, morphology, crystalline orientation and quality, and strain as they have a direct impact on the physicochemical properties of the nanostructures (e.g., optical, electrical, and adsorption characteristics of ions or molecules) [13,14]. Also, for many device applications such as field-effect Transistors (FET) [15], fabrication of two-dimensional (2D) arrays of vertically aligned uniform SiNWs is a preeminent requirement. Considerable efforts have been devoted to developing controlled synthesis of SiNWs by various approaches such as vapor liquid-solid (VLS) growth [16], laser ablation [17], thermal evaporation decomposition [18] and lithography related etching method [19,20]. The VLS technique exploiting metal droplets as catalyst is one of the most prevalent bottom-up methods for the epitaxial growth of SiNWs. These droplets, typically gold, are heated above the Au-Si eutectic point while a background flux of Si, the Au droplets become saturated with Si atoms, and nanowires grow below the droplet. Although relatively well-characterized, the use of this technique faces many challenges, such as metal in-diffusion due to high growth temperature introducing defects and reducing minority carrier lifetime, limiting final device performance. In addition, vertical epitaxial growth of SiNWs on Si (100) wafers, which are conventionally used in current CMOS technology, still remains a challenge due to the preferred growth directions of SiNWs to <111>, <112>, and <110> [21]. Tight control over the diameter and spacing of SiNWs is rather difficult to achieve unless location of metal nanoparticles is lithographically defined on the substrate. In addition to the different bottom-up fabrication methods cited previously, several alternative top-down approaches exist. Using standard silicon processing, a sequence of lithography and etching, often employing electron-beam lithography and reactive ion etching has been considered to fabricate vertical SiNWs out of a silicon wafer. As an alternative to reactive-ion etching, metal-assisted chemical etching (MaCE) [22] of silicon has attracted increasing attention recently. In this approach, silicon is wet-chemically etched under the presence of a noble metal salt in the etching solution which acts as a catalyst to the Si dissolution. MaCE has been successfully applied to produce tilted and zigzag nanowires [23], nanocones [24], helical holes [25], cycloidal [26] and spiral trenches [27]. While this fabrication method has the advantages of simplicity, large scale, and low cost, it does not allow reliable control over wire diameter and spacing inherent in the random distribution of metal particles on the silicon surface by electroless deposition. Yet, programmable assembly of nanowires into ordered arrays is essential for realizing integrated circuits from the synthetic nanowires. The predictable synthesis and controllable assembly of Si nanowires will enable the creation of functional devices. By combining patterned thin metallic layer and catalytic etching large-scale fabrication of SiNW arrays with controlled location can be achieved [28]. During etching, this perforated metal film will etch down into the silicon producing vertical silicon nanowires at the locations of the holes in the metal film.

In this paper, we report on a simple technique to generate large-area silicon nanowire arrays with controlled size, orientation, and packing density with a high throughput by the combination of nanosphere or laser interference lithography and metal-assisted chemical etching.

2 Lithographic approaches to fabricate well-ordered metallic meshes

In order to validate the application of metal-assisted chemical etching to nanostructure-based devices, it is essential to be able to demonstrate a controlled fabrication of Si nanostructures. Metal-assisted etching used in combination with various film-patterning techniques has been employed to fabricate high-aspect-ratio one-dimensional silicon nanostructures including both pore and wire arrays.

In this section, the various lithographic techniques used to create patterned catalyst films are described. The main techniques include nanosphere lithography and laser interference lithography.

Nanosphere lithography (NSL):

Nanosphere lithography, also known as "colloidal lithography" [29], "shadow nanosphere lithography" [30], and "natural lithography" [31] is a cost- and time-effective technique for the fabrication of well-ordered large-area arrays of nanostructures. This method is often considered as a hybrid between the bottom-up approach (due to the self-organization of the colloidal spheres in close packed lattice) and the top-down approach (due to the obtention of dots/structured layers such as in a conventional lithography technique). A typical NSL process involves the following stages in various order (i)

template preparation (ii) template modification (iii) metal/dielectric deposition and (iv) lift-off process [32]. Template preparation is based on a self-assembled array of spheres, which serve as a lithographic mask or template for various subsequent deposition, etching, or imprinting processes [33]. Under appropriate conditions, the disordered colloids form an ordered, stable, and static structure. The disordered system tends to adopt the lowest Gibbs free energy available to them [34]. Consequently, the self-assembly of spherical particles results in hexagonal close-packed (hcp) or face-centered cubic lattices. Thus, nanometer-sized periodic objects with highly symmetrical shapes can be created [35]. The study of NSL can be traced back to 1981, when Fischer and Zingsheim reported the formation of an ordered monolayer on a glass plate [36]. They simply deposited a suspension of colloidal spheres with a diameter of 312 nm and allowed it to evaporate. They obtained small-area particle monolayers. However, the focus of their work was the replication of submicroscopic patterns using visible light and not fabrication of lithographic colloidal masks. A year later, Deckman and Dunsmuir [30] prepared a monolayer of spherical particles by electrostatic adsorption and spin-coating approaches and used it as a lithography template to evaporate nanostructured material through the perforations between spherical particles. In 1995, Hulteen and Duyne renamed the method "nanosphere lithography" [37]. The pioneering works focused on the fabrication of disconnected nano-triangle arrays by vertical metal deposition on nanosphere masks, with the ultimate goal of developing biosensors based on surface enhanced Raman spectroscopy [38]. In 1997, Haginoya et al. introduced a derivative of the classical NSL technique where they demonstrated the fabrication of nanohole arrays by shrinking the size of individual polystyrene (PS) particles while preserving their location in the array using reactive ion etching (RIE) [39].

Our process to fabricate well-ordered metallic mesh consists of five steps being schematically displayed in figure 1. We use 4-inch silicon which is cut into 20 x 20 mm^2 pieces and further cleaned in a RCA solution to remove organics. The resulting hydrophilic chips are then spin-coated with a close-packed monolayer of 400nm silica nanospheres. Subsequently, the size of the silica spheres is reduced by an oxygen plasma RIE process, transferring the close-packed silica spheres into non-close-packed ones. In the next step, a noble nickel – gold metal film with respective thicknesses of 1.5nm and 15nm are deposited by e-beam evaporation onto the Si substrate with the non-close-packed PS sphere as a mask. Finally, the nanospheres are removed by brief ultrasonication in DI water for 3 min. This process results in a continuous layer of noble metal with an ordered hexagonal array of holes. The diameter of the holes is determined by the remaining diameter of the RIE-etched silica spheres.

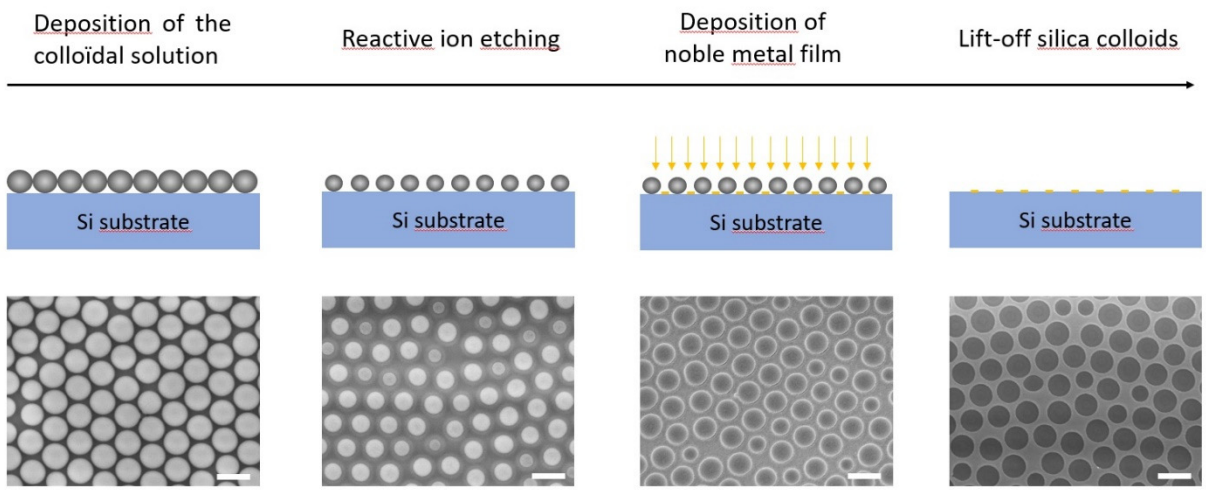

Figure 1 – Overview of the main steps used during the fabrication of the metallic mesh by NSL: A nanosphere monolayer is self-assembled and the size of the silica colloids (400nm originally) can be adjusted by an etching step. The metallic film is then deposited onto the substrate and the nanospheres are removed (scale bars are 500 nm).

Laser Interference Lithography (LIL):

In the fabrication of array of nanosphere masks, defects and domain structures are inevitable. This lithography process repeatedly lacks long range order due to the propensity to nucleate uncorrelated domains on the surface yielding edge defects and small grain boundaries. As a result, it is very difficult to fabricate defect-free Si nanowire arrays using this technology. An alternative method for the fabrication of metallic patterned templates is laser interference lithography where two or more coherent laser beams interfere on a substrate covered with a photoresist film [40]. LIL is a fast, simple and inexpensive, mask-less technique which can be used to fabricate periodic defect free nanostructures with exceptional pattern flexibility and high resolution over large areas [41].

There are two principal configurations for LIL: the Lloyd's mirror interferometer used for high resolution, and the dual beam interferometer, used for large areas. In our experiment, the exposure was carried out using Llyod's mirror setup [42] as it is less sensitive to fluctuations and easier to align (figure 2).

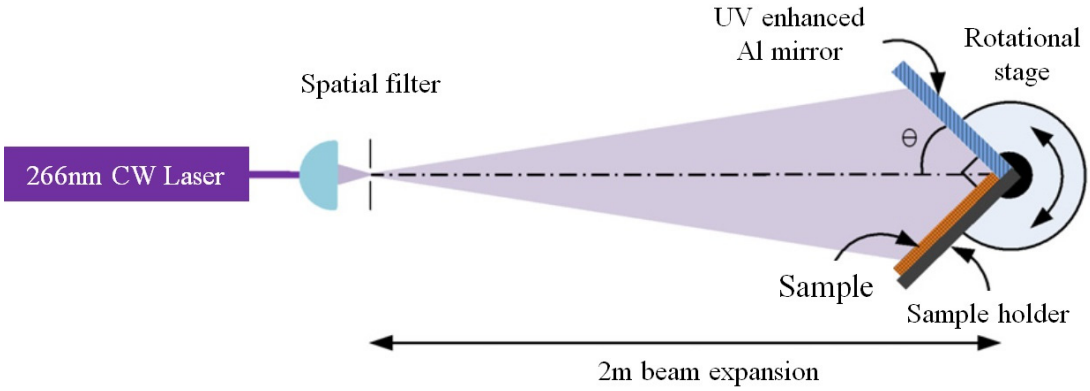

Figure 2 – Schematic of Lloyd's mirror interferometer for laser interference lithography

A 10mW, 266nm UV laser is used as a light source. A spatial filter with an UV objective lens and a 10μm diameter pinhole allows the high frequency noise to be removed from the beam to provide a clean Gaussian profile. The diverging beam travels 2 m over an optical table to a Lloyd's Mirror Interferometer mounted on a rotation stage. The portion of the beam which is reflected off the mirror surface interferes with the part of the beam that is directly incident on the sample (Figure 3a). The interference leads to a standing wave intensity distribution in the photoresist (Figure 3b) with a period $P = \lambda / (2\sin\theta)$, where λ is the wavelength of the laser beams, and θ the half angle at which two beams intersect. The period can therefore be adjusted by changing the angle θ of the rotation stage. After the resist is developed, parallel stripes on the sample surface are present. Mesh-like patterns can be obtained using a double-exposure technique, where after the first exposure the substrate is rotated by 90° and is exposed again.

To start with, Si (100) is cut in 2cm x 2cm chips and cleaned in acetone in an ultrasonic bath. The diced wafers are then rinsed by IPA and a nickel (1nm) – gold (10nm) metal film is deposited by e-beam evaporation (figure 4). A 300nm-thick MaN-2403 negative resist is coated and baked at 90°C for 1min. To prevent the back reflection at the substrate-resist interface, an 200nm-thick anti-reflection coating layer (ARC: AZ-BARLi-II 90) is coated underneath the photoresist layer. The sample is then exposed in the Lloyd's mirror type LIL setup with a double exposure by the 90° sample rotation after the first exposure. The unexposed photoresist is further removed by proper development leaving behind a homogeneous mask with arrays of cylindrical holes. The pattern is subsequently transferred to the ARC layer by RIE in O_2/Ar gas and directional ion milling with argon ions is used to transfer these features to the metallic layer that was deposited underneath the photoresist film. The regions that are not protected by the photoresist are etched away. The remaining photoresist on top is then removed with a gentle oxygen plasma treatment of the surface, resulting in a continuous layer of metal with a perfectly ordered array of holes over a macroscopic area.

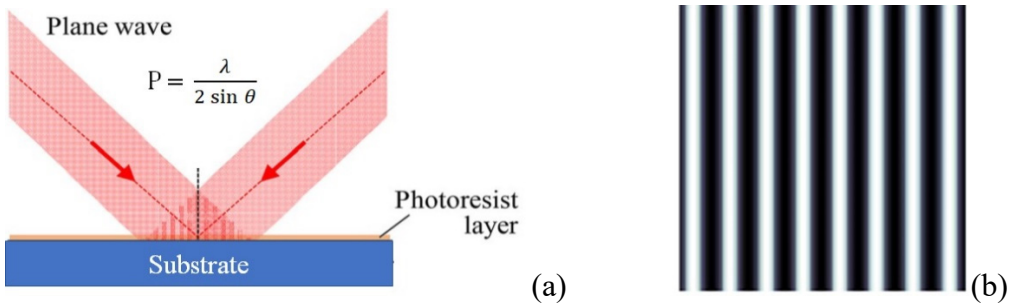

Figure 3 – Interference pattern from a singe exposure: (a) generation of interference fringe patterns. (b) Simulation of line interference pattern for a single exposure (500nm period).

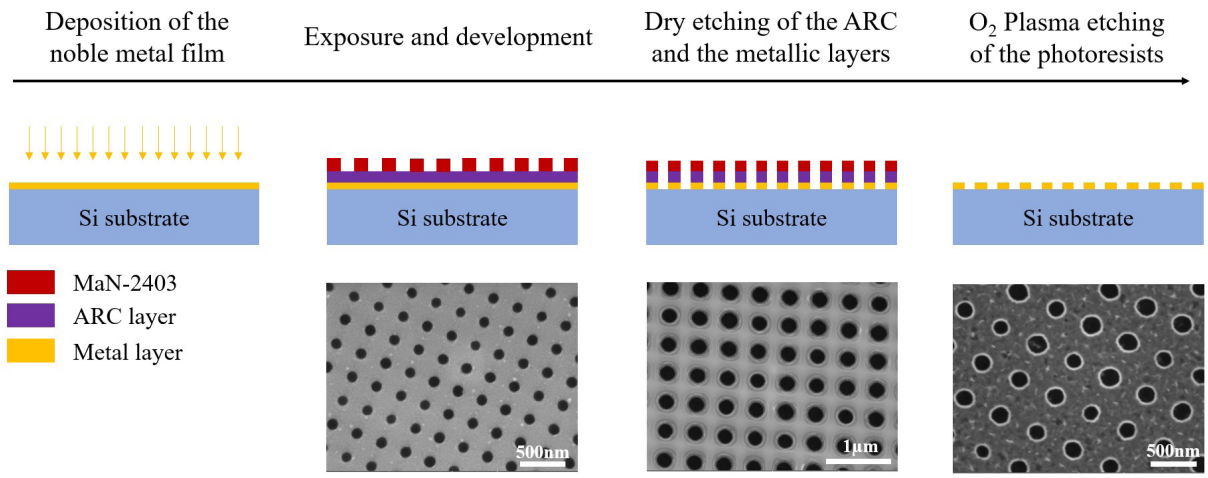

Figure 4 – Overview of the main steps used during the fabrication of the metallic mesh by LIL: A metallic film is first deposited on a silicon substrate. An ARC and photoresist is then exposed by LIL and after development the pattern is successively transferred to the ARC and the metallic layer by dry etching. The polymer layers are finally removed by O_2 plasma etching.

3. Silicon nanowires formation

Principle of metal assisted chemical etching (MACE):

Metal-assisted chemical etching is an alternative to the dry etching method. This is a wet but highly anisotropic process. MACE has recently been applied to fabricate high aspect ratio SiNWs [43], three-dimensional, well-defined nanostructures [44] and porous Si [45]. In MACE, a metal catalyst such as Au, Pt, or Ag is deposited onto a silicon surface either as nanoparticles or a as discontinuous thin film that locally increases dissolution of silicon in an etch solution of hydrofluoric acid (HF) and hydrogen peroxide (H_2O_2). The localized electrochemical reaction with the metal region acting as a microscopic cathode and the metal-semiconductor interface acting as the anode is shown in Figure 5. The oxidant (H_2O_2) used in the etching solution gets reduced locally on the surface of the catalyst where the role of the metal is to reduce the activation energy required for the reduction of the oxidant (gain of electrons). The reduction of the oxidant in the presence of protonated Hydrogen (H^+) coming from the acidic solution (HF) results in the injection of holes into the semiconductor region surrounding the metal layer. The etching rate of the Si underneath the noble metal is much faster than that of the Si without metal coverage [46]. Therefore, the noble metal sinks into the Si substrate producing a high aspect ratio structure without net consumption of the noble metal. The pattern of the noble metal thus can be engraved into the Si substrate to produce nanostructures [47]. Hence, as a wet etching process without high energy ions involved, MACE relieves the lattice damage from dry etching process and eliminates the etching depth limitations for features with small lateral dimensions [48].

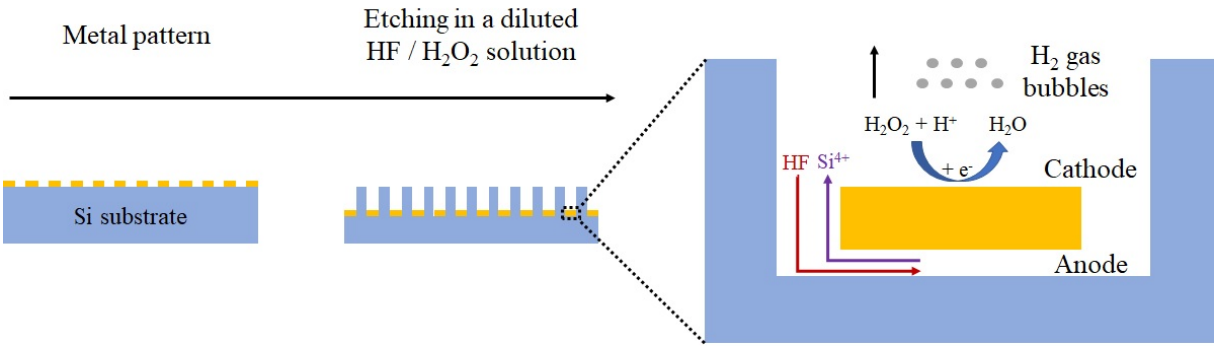

Figure 5 – Schematic illustration of the metal-assisted chemical etching of Si in diluted HF/H_2O_2 diluted solution.

In the current work gold was used as a catalytic metal. The surface of the gold facing the etching solution acts as the cathode (figure 5), which catalyzes H_2O_2 reduction, consuming H and electrons (e^-). It could be described by the following reactions:

At the cathode:

$H_2O_2 + 2H^+ \rightarrow 2H2O + 2h+$ (local reduction)
$2H^+ \rightarrow H2 + 2h+$ (hydrogen gas formation)

The surface of the gold facing the Si works as the anode and catalyzes Si oxidation, generating H and e-, which is described as:

At the anode:

$Si + 6HF + 4h+ \rightarrow H2SiF6 + 4H+$
(oxidation and dissolution of Si)

The overall reaction could be written in the following way:

Net reaction:

$Si + 6HF + H2O2 \rightarrow H2SiF6 + 2H2O + H2$

Unlike wet chemical etching, the metal layer sinks to the bottom and travels along with the semiconductor which helps to achieve higher aspect ratios and novel surface morphologies. The lateral dimension of the structure formed is limited by the dimension of the metal mesh made using lithography and the vertical dimension is controlled by the etch time.

Metal-assisted Si etching depends on several parameters, for instance:

- the type of deposited metal (Pt, Ag, Au, etc.)
- the dopant type and doping level (n- or p-type)
- etching time, temperature of etching and ambient illumination
- concentration of etchants (HF, H_2O_2, dilution)
- wafer orientation (<100>, <111>, <110>, <113>)
- morphology of the metal film (single particles, discontinuous or continuous film)

Therefore, Si structures with different morphologies and properties can be produced by varying these parameters.

Ordered silicon nanowire arrays fabrication:

The Si nanowires are formed by immersing the gold mesh-loaded silicon substrate in a solution of [HF (5 M) : H_2O_2 (30%)] = 10 : 1 at room temperature and ambient illumination. Under these conditions, the silicon is selectively and anisotropically etched under the gold at the rate of 700 nm/min leaving behind a well-ordered array of vertically standing SiNWs (figure 6). Our samples are typically etched less than 5min to create up to 4μm in length.

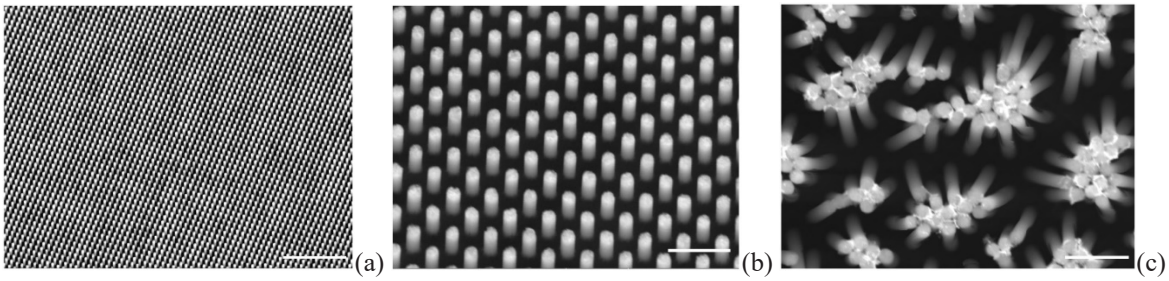

Figure 6 – SEM images of SiNW array after the anisotropic wet etching process (scale bars are 5μm and 1μm respectively for figure 6a and 6b). SiNWs sticking together during the drying process (figure 6c, scale bare is 1μm).

5. Discussion

The method enables control of the diameter in a wide range, from ~100nm to ~600nm. The length of Si nanowires varies linearly with the etching time, allowing easy control of their length. The upper parts of nanowires may be bent and stuck together if the Si nanowires have a relatively large aspect ratio (ratio of length to diameter) and a high surface density (figure 6c). The nanowires tend to form bundles of nanowires. The formation of bundles of nanowires is attributed to surface tension forces exerted on the nanowires during the drying of the sample, which is a common phenomenon for drying of long nanowire arrays from the solvent. This can be prevented with super-critical CO_2 drying.

4. Conclusion

In summary, large-area vertically ordered silicon nanowire arrays have been fabricated with low-cost and high throughput by a catalytic templated etching process. A combination of 2D non-close-packed silica colloidal crystal template or laser interference lithography to create a gold nanohole array on a silicon substrate and metal-assisted chemical etching, a wet but directional etching process, can produce high aspect ratio silicon nanowires with controlled diameter, length, and density. Since the etching step takes place at room temperature, no metal impurities should be incorporated in the core of the nanowires, and surface contamination can be removed. Further, surface damage should not be a concern as no high energy ions are involved in the process. The vertically ordered silicon nanowires synthesized by the current method may find multiple applications in array devices, such as field-effect transistors, sensors, electrodes, and two-dimensional photonic crystals.

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